WHAT IS CLAIMED IS:

1. A data memory circuit, comprising:

a plurality of addressable memory cells;

a command-decoding device for decoding external commands;

a control device for controlling and initiating operations on the memory cells in response to the decoded commands; and

a command buffer device for buffer-storing a command received in a critical operating state period during which execution of the command is impermissible and for releasing the command for execution after end of the critical operating state period.

2. The data memory circuit of claim 1, wherein a plurality of critical operating states are possible, and in one or more critical operating states, a set of commands is impermissible; and wherein the command buffer device includes a buffer circuit assigned to each individual command of the set of impermissible commands.

3. The data memory circuit of claim 2, wherein each buffer circuit comprises:

a state evaluation circuit for generating a buffer standby signal during at least one operating state that is critical for the execution of respective impermissible command; and

a logic circuit for setting a bi-stable element into a first state when the assigned command appears while the buffer standby signal is active and for re-generating the assigned command after the buffer standby signal has ended.

4. The data memory circuit of claim 3, wherein the command decoding device comprises:

a predecoder, which, for each received command, activates a command line assigned to the received command; and

an end decoder which excites selected enable lines of the control device depending on which of the command lines is activated; and wherein each buffer circuit is connected to a respectively assigned command line between the

predecoder and the end decoder to receive the command from respective command line and to apply a re-generated command generated to respective command line.

5. The data memory circuit of claims 4, wherein each buffer circuit includes a switch in a path of the respective command line, wherein the switch is opened precisely while a buffer standby signal is active to inhibit forwarding of an activation of the command line effected by the predecoder to the end decoder.

6. The data memory circuit of claim 5, wherein a source of external commands is adapted to a specification of the data memory circuit with regard to command-issuing times, and wherein the command buffer device handles external commands whose execution leads to termination of internally controlled processes in the data memory circuit.

7. The data memory circuit of claim 6, wherein the command buffer device handles external commands whose execution leads to termination of a self-controlled data-refresh process in the memory circuit.

8. The data memory circuit of claim 1, wherein the control device includes blockage elements for blocking execution of commands during the critical operating state period, and wherein the command buffer device directly forwards commands received during the critical operating state period.

9. The data memory circuit of claim 1, wherein the command buffer device inhibits forwarding of the received command to the control device during the critical operating state period.

10. A data memory circuit, comprising:

a plurality of addressable memory cells;

a command decoder for receiving commands, the command decoder having a plurality of command-buffer circuits for buffer-storing commands received during critical operation state periods when execution of the commands is impermissible

and for releasing the buffer-stored commands for execution after the critical operation state periods; and

an internal controller for controlling operations on the memory cells in response to commands from the command decoder.

11. The data memory circuit of claim 10, wherein the command decoder further comprises:

a predecoder;

an end decoder; and

a plurality of command lines connecting the plurality of command-buffer circuits between the predecoder and the end decoder, wherein the predecoder assigns and activates one or more command lines in response to the received commands and the end decoder excites one or more enable lines of the internal controller corresponding to the activated command lines.

12. The data memory circuit of claim 11, wherein each command-buffer circuit comprises:

a state evaluation circuit for generating a buffer standby signal during the critical operation state periods; and

a logic circuit for holding an assigned command while the buffer standby signal is active and for forwarding the assigned command to the end decoder after the buffer standby signal has ended.

13. The data memory circuit of claim 12, wherein each command-buffer circuit further comprises a switch disposed in-line with the respective command line connecting the predecoder and the end decoder, wherein the switch is connected to the state evaluation circuit and opens when the buffer standby signal is active.

14. The data memory circuit of claim 12, wherein the internal controller includes a command-blocking circuit for blocking execution of commands during the critical operation state periods.

15. The data memory circuit of claim 12, wherein the command buffer circuits handle external commands whose execution leads to termination of internally controlled processes in the data memory circuit.

16. The data memory circuit of claim 12, wherein the command buffer circuits handle external commands whose execution leads to termination of a self-controlled data-refresh process in the memory circuit.

17. A data memory circuit, comprising:

a plurality of addressable memory cells;

a decoder means for receiving and decoding commands, the decoder means having a plurality of command-buffer means for buffer-storing commands received during critical operation state periods when execution of the commands is impermissible and for releasing the buffer-stored commands for execution after respective critical operation state periods; and

a controller means for controlling operations on the memory cells in response to commands from the decoder means.

18. The data memory circuit of claim 17, wherein the decoder means further comprises a plurality of command lines connecting the plurality of command-buffer means between a predecoder means for assigning and activating one or more command lines in response to the received commands and an end decoder means for activating one or more enable lines of the controller means corresponding to the activated command lines.

19. The data memory circuit of claim 18, wherein each command-buffer means comprises:

a state evaluation means for evaluating an operating state of the memory cells and for generating a buffer standby signal during the critical operation state periods; and

a logic circuit means for holding an assigned command while the buffer standby signal is active and for forwarding the assigned command to the end decoder after the buffer standby signal has ended.

20. The data memory circuit of claim 19, wherein each command-buffer means further comprises a switching means for selectively opening and closing the respective command line, the switching means disposed in-line with the respective command line connecting the predecoder means and the end decoder means, wherein the switching means is connected to the state evaluation circuit and opens when the buffer standby signal is active.

21. A method for controlling the execution of commands in a memory device comprising a plurality of addressable memory cells, the method comprising:

receiving an external command while the memory device is performing a critical operation making execution of the external command impermissible;

buffering the external command until the device completes the critical operation; and then

executing the command.